The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse.

When the clock input is at either the high or low level, the D input signal has no effect at the output.

EFUNCTION TABLE

Inputs Outpu						
Clear	Clock	D	Q			
L	×	×	L			
H	1	Н	Н			
Н	t	L	L			
Н	L	×	Q_o			

Notes;

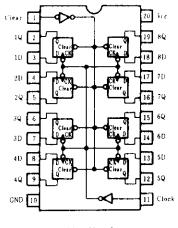
H = high level, L = low level,

X = irrelevant

t = transition from low to high level Q₀ = level of Q before the indicated steady-state input conditions

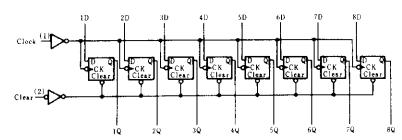
were established.

MPIN ARRANGEMENT



(Top View)

BBLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item Supply voltage		Symbol	min	typ	max	Unit	
		Vci	4.75	5.00	5.25	V	
Output current Clock frequency		Іон	_		-400	μA	
		Iot			8	mA	
		f.clock	0		30	MHz	
Clock	and clear pulse width	t w	20		_	ns	
Setup	Data		20 t	_			
time	Clear inactive-state	1 ***	25 †		_	ns	
Data h	old time	t h	5 †		_	ns	

Note) † : The arrow indicates the rising edge of clock pulse.

ELECTRICAL CHARACTERISTICS $(Ta = -20 \sim +75^{\circ}C)$

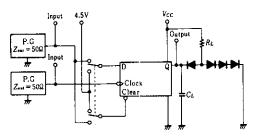
Item	Symbol	Test Conditions		min	typ⁴	max	Unit
	VIH			2.0	_		V
Input voltage	VIL			-		0.8	V
	Von	$V_{CC}=4.75V$, $V_{IB}=2V$, $V_{IL}=0.8V$, $I_{OB}=-400\mu$ A		2.7			V
Output voltage		$V_{CC}=4.75V, V_{IH}=2V,$	Io1 -8mA	_		0.5	V
	1 Vor	$V_{IL}=0.8V$	IoL -4mA			0.4	l
	I,	$V_{cc} = 5.25 \text{V}, V_i = 7 \text{V}$				0.1	mА
	I _{IH}	$V_{cc} = 5.25 \text{V}, V_l = 2.7 \text{V}$	_	_	20	μΑ	
	In	$V_{cc} = 5.25 \text{V}, V_t = 0.4 \text{V}$				-0.4	mΑ
Short-circuit output current	Ins	$V_{CC} = 5.25 \text{V}$	-20		-100	mA	
Supply current	Icc**	$V_{cc} = 5.25 \text{V}$	_	17	27	mA	
Input clamp voltage	VIK	$V_{CC} = 4.75 \text{V}, I_{IN} = -18 \text{m}$		_	-1.5	V	

^{*} VCC=5V, Ta=25°C

ESWITCHING CHARACTERISTICS $(V_{cc}=5V, T_a=25^{\circ}C)$

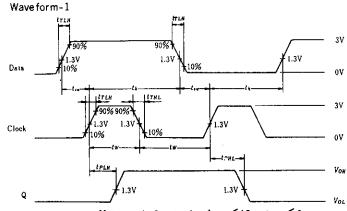
Item	Symbol	Inputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	∫mex.	Clock		30	<u> </u>		MHz
Propagation Delay Time	t _{PHL}	Clear	$C_L = 15 \text{pF}, R_L = 2 \text{k}\Omega$		18	27	ns
	1 PLH			-	17	27	
	1 PHL	Clock		_	18	27	1

■TESTING METHOD

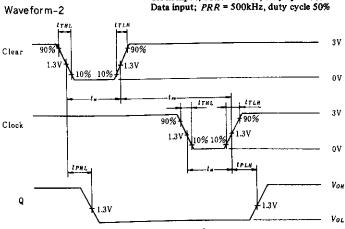


Notes:

- 1. C_L includes probe and jig capacitance. 2. All diodes are 1S2074 lacktriangle.



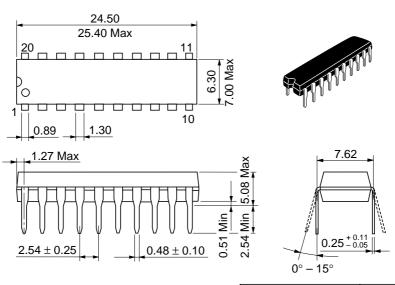
 Input pulse; t_{TLH} ≤ 15ns, t_{TLH} ≤ 6ns Clock input; PRR = 1MHz, duty cycle 50% Notes:



Note: Input pulse; $t_{TLH} \le 15$ ns, $t_{THL} \le 6$ ns, PRR = 1MHz.

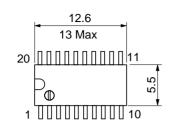
With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

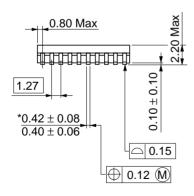
Unit: mm

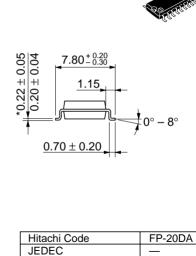


Hitachi Code	DP-20N
JEDEC	_
EIAJ	Conforms
Weight (reference value)	1.26 g

Unit: mm







Weight (reference value)

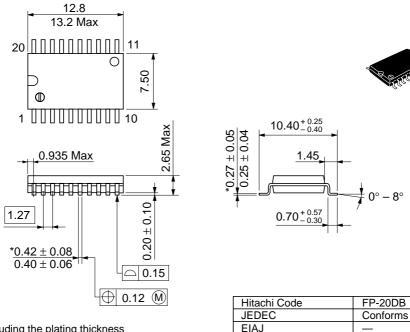
Conforms

0.31 g

EIAJ

*Dimension including the plating thickness
Base material dimension

Unit: mm



Weight (reference value)

0.52 g

*Dimension including the plating thickness
Base material dimension

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