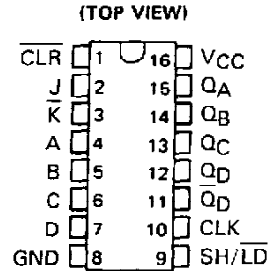


**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195**
4-BIT PARALLEL-ACCESS SHIFT REGISTERS
MARCH 1974—REVISED MARCH 1988

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and \bar{K} Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High Performance: Accumulators/Processors Serial-to-Parallel, Parallel-to-Serial Converters

SN54195, SN54LS195A, SN54S195 . . . J OR W PACKAGE
SN74195 . . . N PACKAGE
SN74LS195A, SN74S195 . . . D OR N PACKAGE



description

These 4-bit registers feature parallel inputs, parallel outputs, J- \bar{K} serial inputs, shift/load (SH/ \bar{L}_D) control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

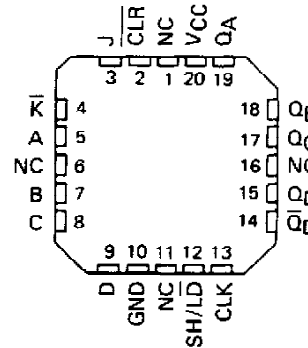
Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking SH/ \bar{L}_D low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when SH/ \bar{L}_D is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs permit the first stage to perform as a J- \bar{K} , D-, or T-type flip-flop as shown in the function table.

The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

SN54LS195, SN54S195 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'S195	105 MHz	350 mW

FUNCTION TABLE

CLEAR	SHIFT/ LOAD	CLOCK	INPUTS				OUTPUTS						
			SERIAL J	SERIAL \bar{K}	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
L	X	X	X	X	X	X	X	L	L	L	L	H	
H	L	↑	X	X	a	b	c	d	a	b	c	d	\bar{d}
H	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\bar{Q}_{D0}	
H	H	↑	L	H	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	
H	H	↑	L	L	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	
H	H	↑	H	H	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	
H	H	↑	H	L	X	X	X	\bar{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	

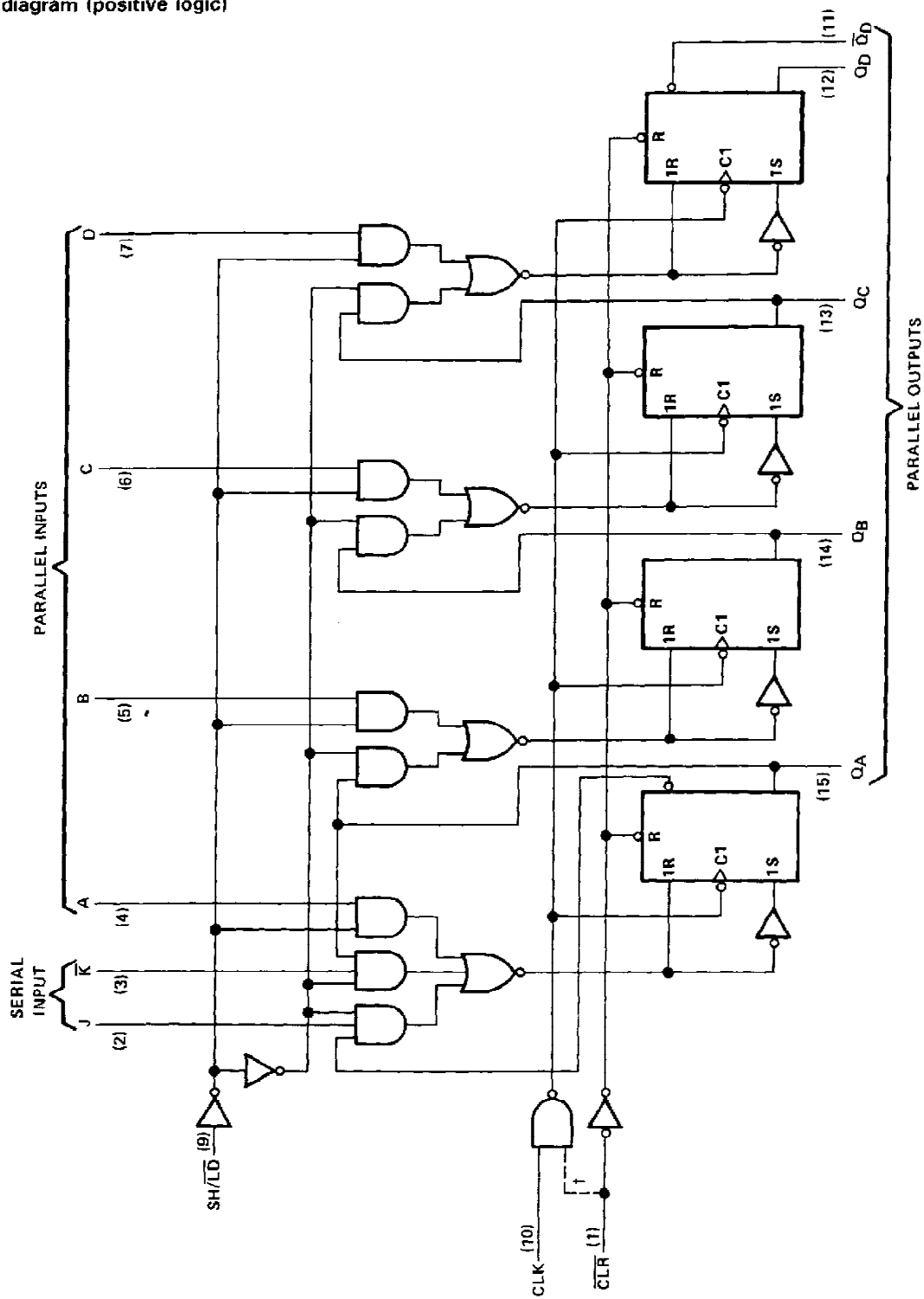
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of Q_A, Q_B, Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established
 Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B , or Q_C , respectively, before the most-recent transition of the clock

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**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

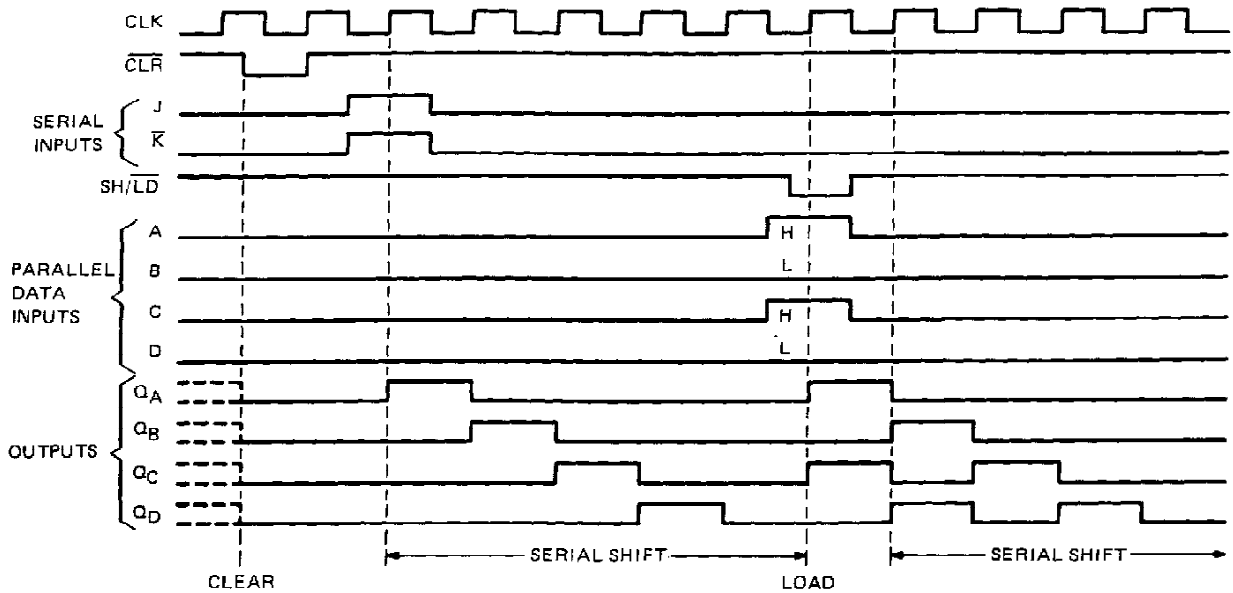
logic diagram (positive logic)



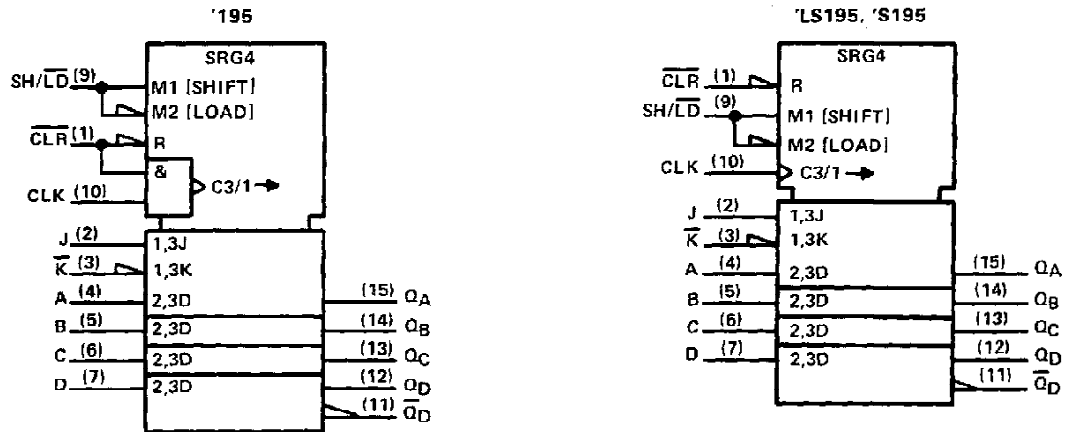
† This connection is made on '195 only.
Pin numbers shown are for D, J, N, and W packages.

**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

typical clear, shift, and load sequences



logic symbols†

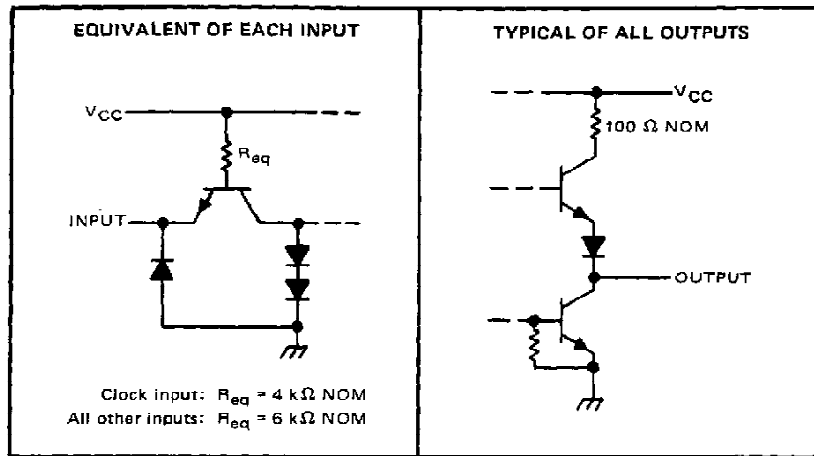


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers are for D, J, N, and W packages.

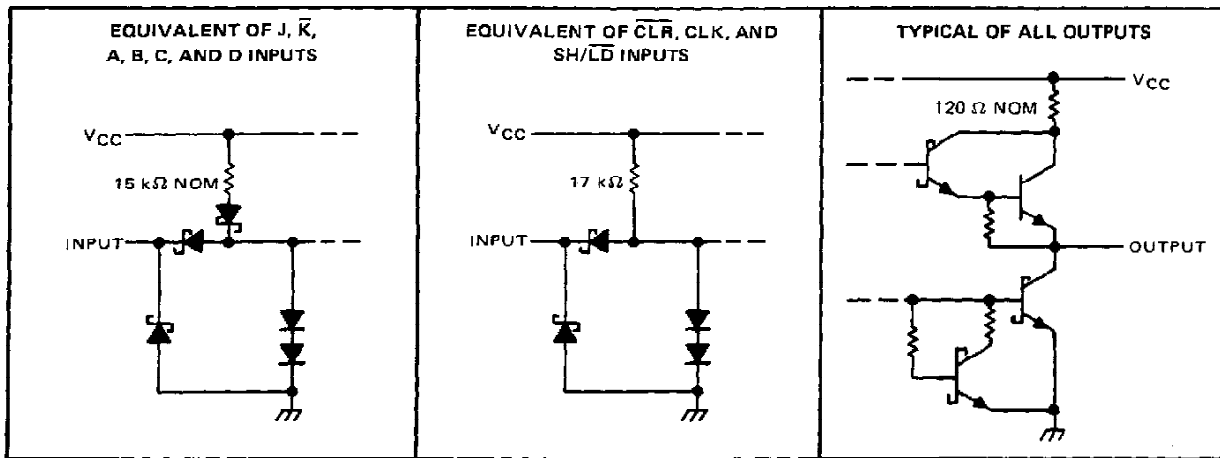
SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

schematics of inputs and outputs

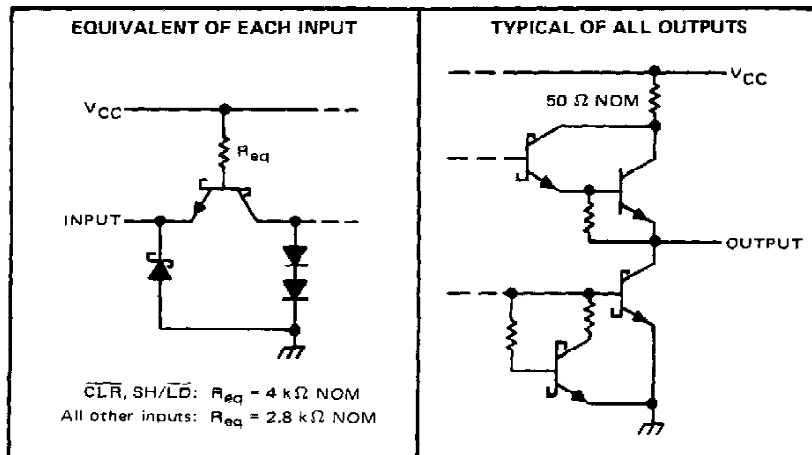
'195



'LS195A



'S195



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SN54195, SN74195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54195	-55°C to 125°C
SN74195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54195			SN74195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock input pulse, $t_w(\text{clock})$	16			16			ns
Width of clear input pulse, $t_w(\text{clear})$	12			12			ns
Setup time, t_{SU} (see Figure 1)	Shift/load	25		25			ns
	Serial and parallel data	20		20			
	Clear inactive-state	25		25			
Shift/load release time, $t_{release}$ (see Figure 1)			10			10	ns
Serial and parallel data hold time, t_H (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54195	-20	-57	mA
		SN74195	-18	-57	
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		39	63	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§]Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, \bar{K} , and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1	30	39		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns



SN54LS195A, SN74LS195A

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS195A	-55°C to 125°C
SN74LS195A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS195A			SN74LS195A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock or clear pulse, $t_w(\text{clock})$	16			16			ns
Width of clear input pulse, $t_w(\text{clear})$	12			12			ns
Setup time, t_{SU} (see Figure 1)	Shift/load			25			ns
	Serial and parallel data			15			
	Clear inactive-state			25			
Shift/load release time, $t_{release}$ (see Figure 1)			10			20	ns
Serial and parallel data hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS195A			SN74LS195A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$			0.25	0.4		0.25	0.4
	$I_{OL} = 4 \text{ mA}$						0.35	0.5
	$I_{OL} = 8 \text{ mA}$							
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		14	21		14	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figure 1	30	39		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns


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SN54S195, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S195	-55°C to 125°C
SN74S195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S195			SN74S195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Clock frequency, f_{clock}	0		70	0		70	MHz
Width of clock input pulse, $t_w(\text{clock})$	7			7			ns
Width of clear input pulse, $t_w(\text{clear})$	12			12			ns
Setup time, t_{su} (see Figure 1)	Shift/load	11		11			ns
	Serial and parallel data	5		5			
	Clear inactive-state	9		9			
Shift/load release time, $t_{release}$ (see Figure 1)			2			6	ns
Serial and parallel data hold time, t_h (see Figure 1)	3			3			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage			2			V
V_{IL} Low-level input voltage					0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S195	2.5	3.4		V
		SN74S195	2.7	3.4		
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$				0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				50	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$				-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$		-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54S195		70	99	mA
		SN74S195		70	109	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

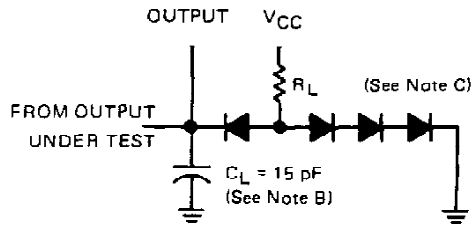
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Figure 1	70	105		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			11	16.5	ns


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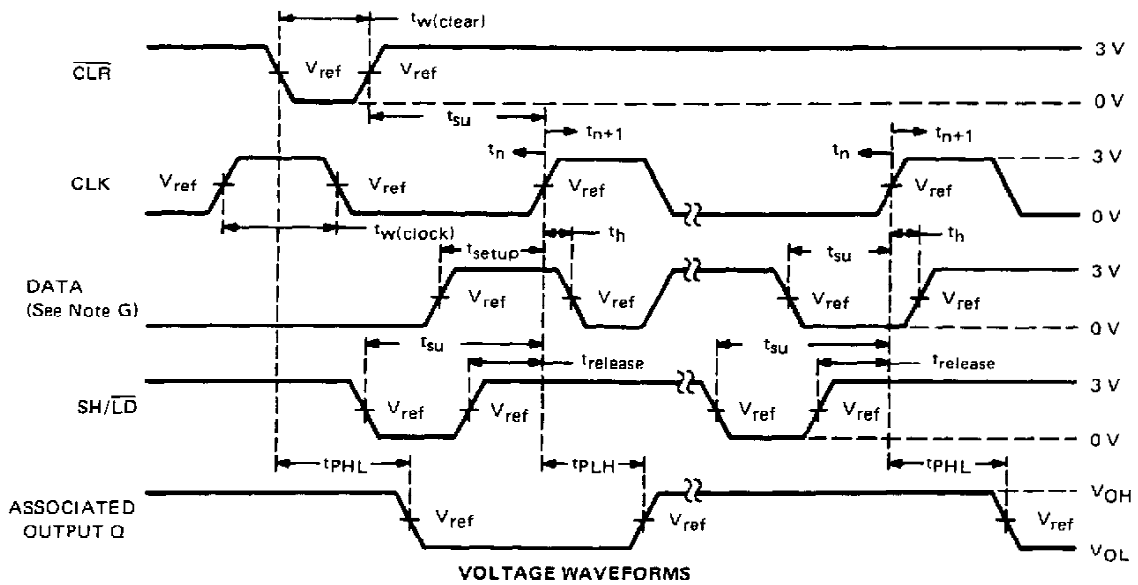
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**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



- NOTES:**
- A. The clock pulse generator has the following characteristics: $Z_{OUT} \approx 50 \Omega$ and $PRR \leq 1 \text{ MHz}$. For '195, $t_r \leq 7 \text{ ns}$ and $t_f \leq 7 \text{ ns}$. For 'LS195A, $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. For 'S195, $t_r = 2.5 \text{ ns}$ and $t_f = 2.5 \text{ ns}$. When testing f_{max} , vary the clock PRR.
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N3064 or equivalent.
 - D. A clear pulse is applied prior to each test.
 - E. For '195 and 'S195, $V_{ref} = 1.5 \text{ V}$; for 'LS195A, $V_{ref} = 1.3 \text{ V}$.
 - F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
 - G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
 - H. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

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